

CLAIMS

- 1 1. A message writing apparatus characterized by comprising:
2 receiving means (21b) for receiving cells having path
3 information, said cells being obtained by division of a
4 variable-length message;
5 message area allocating means (21e) for extracting said
6 path information from the received cells received by said
7 receiving means (21b) to allocate a memory area (22)
8 corresponding to said path information, said memory area (22)
9 being larger than a size of said variable-length message;
10 writing ranking adding means (23) for adding writing
11 ranks to the received cells when the received cells are written
12 in said memory area (22) allocated by said message area
13 allocating means (21e); and
14 storing means (25) for writing the received cells in
15 said memory area (22) according to said writing ranks added
16 by said writing rank adding means (23).
- 1 2. A message writing apparatus according to claim 1,
2 characterized in that said message area allocating means (21e)
3 includes:
4 address table setting means for setting, in said memory
5 area (22), an address table area (23) in which a size of a
6 writing area, a writing position of said variable-length
7 message and the number of received cells, corresponding to
8 said path information, are related to each other on the basis

9 of cell numbers and message number of the received cells;
10 and

11 message storing area setting means for setting, in said
12 memory area (22), a message storing area (24) which CPU reads
13 out the received cells in message units.

1 3. A message writing apparatus according to claim 1,
2 characterized in that said writing rank adding means (23)
3 is made to add said writing ranks to said received cells in
4 the order of receiving processing of the received cells.

1 4. A message writing apparatus according to claim 1,
2 characterized in that said writing rank adding means (23)
3 is made to add said writing ranks to said received cells by
4 writing flag information indicative of whether or not the
5 received cells are read out, in flag areas (K1, ..., Ka) placed
6 in said memory area (22).

1 5. A message writing apparatus according to claim 4,
2 characterized in that said writing rank adding means (23)
3 is equipped with residual quantity examining means (K₂₋₁, ...,
4 K_{2-n}) for checking said flag information to examine a size
5 of a free area for writing of the received cells.

1 6. A message writing apparatus according to claim 1,
2 characterized in that said writing rank adding means (23)
3 is made to add said writing ranks by reading out an indication
4 of a head address holding section (40a, 40b) which manages
5 writing positions for writing of the received cells in said

6 memory area (22) and an indication of a message storing/holding
7 section (41a, 41b, 41c) which manages a message number of
8 the written received cells and writing position information.

1 7. A message writing apparatus according to claim 6,
2 characterized in that said writing rank adding means (23)
3 is equipped with residual quantity checking means (K_{2-1} , ..., K_{2-n})
4 for examining a size of a free area for writing of the
5 received cells by checking the indication of said head address
6 holding section (40a, 40b) and the indication of said message
7 storing/holding section (41a, 41b, 41c).

1 8. A message writing apparatus according to any one of claims
2 1 to 7, characterized in that said message is an adaptation
3 layer message and said cells are obtained by division of said
4 adaptation layer message.

1 9. A message writing apparatus according to claim 8,
2 characterized in that said adaptation layer is based on AAL5.

1 10. A message writing method characterized by comprising:
2 a receiving step of receiving cells having path
3 information, said cells being obtained by division of a
4 variable-length message;
5 a message area allocating step of extracting said path
6 information from the received cells received in said receiving
7 step to allocate a memory area (22) corresponding to said
8 path information, said memory area (22) being larger than
9 a size of said variable-length message;

10 a writing rank adding step of adding writing ranks to
11 the received cells when the received cells are written in
12 said memory area (22) allocated in said message area allocating
13 step; and

14 a storing step of writing the received cells in said
15 memory area (22) according to said writing ranks added in
16 said writing rank step.

1 11. A message readout apparatus (20) which reads out each
2 of a plurality of cells constituting a message and written
3 in a memory area (22), characterized by comprising:

4 first means (22, 25) for reading out said message in
5 accordance with writing ranks added in the order of receive
6 processing of said cells;

7 second means (22, 25) for reading out said message on
8 the basis of the added writing ranks in a manner that flag
9 information, indicative of whether or not said cells are read
10 out, is written in said memory area (22);

11 third means (22, 25) for reading out said message on
12 the basis of said writing ranks based on an indication of
13 a message storing/holding section (41a, 41b, 41c) which
14 manages a message number of the received cells written in
15 said memory area and writing position information thereon;
16 and

17 control means (23) operable of selecting any one of said
18 first means (22, 25), said second means (22, 25) and said
19 third means (22, 25) by setting of said memory area (22).

1 12. A message readout apparatus according to claim 11,
2 characterized in that said message is an adaptation layer
3 message and said cells, said cells being obtained by division
4 of said adaptation layer message.

1 13. A message readout apparatus according to claim 12,
2 characterized in that said adaptation layer is based on AAL5.

1 14. A message readout method of reading out each of a plurality
2 of cells constituting a message and written in a memory area
3 (22), characterized by comprising:

4 a first step of reading out said message in accordance
5 with writing ranks added in the order of receive processing
6 of said cells;

7 a second step of reading out said message on the basis
8 of the added writing ranks in a manner that flag information,
9 indicative of whether or not the cells are read out, is written
10 in said memory area (22); and

11 a third step of reading out said message in accordance
12 with said writing ranks provided by an indication of a message
13 storing/holding section (41a, 41b, 41c) which manages a
14 message number of the received cells written in said memory
15 area (22) and writing position information,

16 with any one of said first means, said second means and
17 said third means being selectively implemented according to
18 setting of said memory area (22).

1 15. A memory address control circuit for writing of a

2 variable-length message, characterized by comprising:
3 a path recognizing section (21a) for receiving cells,
4 said cells being obtained by division said variable-length
5 message and transmitted to extract path information from the
6 received cells;
7 a receive control section (21c) operable of adding
8 writing ranks on writing in a memory (22) in correspondence
9 with said path information outputted from said path
10 recognizing section (21a) and of outputting a size of a writing
11 area, a writing position of said variable-length message and
12 the number of received cells as management information;
13 a received message assembling section (21b) having an
14 address table (23), in which said size of said writing area,
15 said writing position of said variable-length message and
16 the number of received cells, corresponding to said path
17 information, are related to each other on the basis of said
18 management information from said receive control section and
19 operable of assembling the received cells with respect to
20 one variable-length message and outputting second write
21 information; and
22 a memory control section (21e) operable of controlling
23 writing in said memory (22) on the basis of said management
24 information from said received message assembling section
25 (21b) and the second write information from the receive control
26 section (21c).

1 16. A memory address control circuit for readout of a

2 variable-length message, characterized by comprising:

3 a path recognizing section (21a) for receiving cells,
4 said cells being obtained by division of said variable-length
5 message and transmitted to extract path information from the
6 received cells;

7 a receive control section (21c) operable of adding
8 writing ranks on readout from a memory (22) in correspondence
9 with said path information outputted from said path
10 recognizing section (21a) and of outputting a size of a readout
11 area, a readout position of said variable-length message and
12 the number of received cells as management information;

13 a received message assembling section (21b) having an
14 address table (23), in which said size of said readout area,
15 said readout position of said variable-length message and
16 the number of received cells being corresponding to said path
17 information, are related to each other on the basis of said
18 management information from said receive control section
19 (21c) and operable of assembling the received cells with
20 respect to one variable-length message to output and
21 outputting second readout information; and

22 a memory control section (21e) operable of controlling
23 the readout to said memory (22) on the basis of said management
24 information from said received message assembling section
25 (21b) and said second readout information from said receive
26 control section.